Docket No.: 50090-265

**PATENT**

#9 Response
M. Brunson
2/5/03

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| In re Application of | : | |
| Kiyotoshi UEDA, et al. | : | |
| Serial No.: 09/766,845 | : | Group Art Unit: 2829 |
| Filed: January 23, 2001 | : | Examiner: P. Patel |

For: METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT MANUFACTURED THEREBY

## RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
Washington, DC 20231

Sir:

Noting the Office Action of January 2, 2003 wherein restriction has been required, Applicant(s) hereby provisionally elect Group I (claims 1-5 and 13) for prosecution in the above-identified application, with traverse.

## REMARKS

MPEP § 811 states that the Examiner "should make a proper requirement as early as possible in the prosecution, in the first action if possible, otherwise, as soon as the need for a proper requirement develops." In the first action, the Examiner made a requirement to restrict between species, to which the Applicants elected without traverse. After Examining the claims on the merits and issuing a non-final Office Action, to which the Applicants duly responded, the Examiner has made another restriction requirement. It is not clear how the need to restrict has developed since the previous response.